Research highlights

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High speed testing circuits are designed to test high speed circuits.

1) A 4 outputs half-rate $2^5$-1 PRBS generator architecture is designed to test high speed transmitters that uses 15% less building blocks as compared to conventional architecture.

2) A distributed XOR gate is designed to solve the problem of multiple XOR gates in critical path of high speed digital circuits.

3) Design of state of the art PLL and CDR circuits is in progress.

Publications: Yet to submit.

Relevant images/ pictures/illustrations.